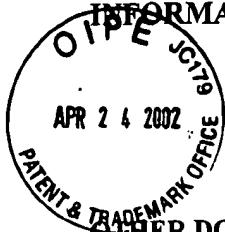


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OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

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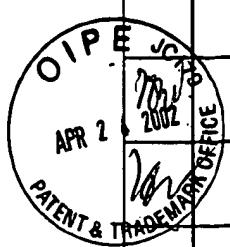
✓	R. Voorakaranam & A. Chatterjee, "Test Generation for Accurate Prediction of Analog Specifications," IEEE VLSI Test Symposium (2000) 137-142. (No month)
✓	J.H. Friedman, "Multivariate Adaptive Regression Splines," The Annals of Statistics, Vol. 19, No. 1, 1-141. (No month)
✓	P.A. Variyam and A. Chatterjee, "Specification-Driven Test Design for Analog Circuits," International Symposium on Defect and Fault Tolerance in VLSI Systems (1998) 335-340. (No month)
✓	T. Wilson, "Test Challenges for Next-Generation RF Devices," EE Evaluation Engineering, Vol. 39, No. 11 (2000) 31-37. (No month)
✓	D.A. Coley, An Introduction to Genetic Algorithms for Scientists and Engineers, World Scinetific (1996) 1-16. (No month)
✓	Cadence SpectreRF Simulator User Guide (December 1999), 16 pages.
✓	Cadence OCEAN Reference Guide (December 1999), 18 pages.
✓	RF Micro-Devices, Low Noise Amplifier/Mixer (March 2001), 6 pages.
✓	S. Cherubal & A. Chatterjee, "Parametric Fault Diagnosis for Analog Systems Using Functional Mapping," Proceedings, Design, Automation and Test in Europe (1999) 195-200. (No month)
✓	P.N. Variyam & A. Chatterjee, "Enhancing Test Effectiveness for Analog Circuits Using Synthesized Measurements," VLSI Test Symposium (1998) 132-137. (No month)
✓	A. Walker, W. Alexander & P.K. Lala, "Fault Diagnosis in Analog Circuits Using Element Modulation," IEEE Design and Test of Computers (March 1992) 19-29.
✓	H. Walker & S.W. Director, "VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits," IEEE Transactions on Computer-Aided Design (October 1986) 541-556.
✓	N.Nagi, A. Chatterjee, A. Balivada & J.A. Abraham, "Fault-Based Automatic Test Generation for Linear Analogy Devices," Proceedings, International Conference on Computer-Aided Design (1993) 88-91. (No month)
✓	M. Salamani & B. Kaminska, "Multifrequency Analysis of Faults in Analog Circuits," IEEE Design and Test of Computers (1995) 70-80. (No month)
✓	B. Hamida, K. Saab, D. Marche, B. Kaminska & G. Qusnel, "LIMSoft: Automated Tool for Design and Test Integration of Analog Circuits," International Test Conference (1996) 571-580. (No month)
✓	H.H. Zheng, A. Balivada & J.A. Abraham, "A Novel Test Generation Approach for Parametric Faults in Linear Analog Circuits," VLSI Test Symposium (1996) 470-475. (No month)

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APR 25 2002

RECEIVED



		A. Balivada, J. Chen & J.A. Abraham, "A Novel Test Generation Approach for Parametric Faults in Linear Analog Circuits," VLSI Test Symposium (1996) 470-475.
		A. Abderrahman, E. Cerny & B. Kaminska, "CLP-Based Multifrequency Test Generation for Analog Circuits," VLSI Test Symposium (1997) 158-165. (No month)
		G. Devarayanadurg & M. Soma, "Dynamic Test Signal Design for Analog ICs," Proceedings, International Conference on Computer-Aided Design (1995) 627-629. (No month)
		W. Verhaegen, G. Van de Plas & G. Gielen, "Automated Test Pattern Generation for Analog ICs," Proceedings, VLSI Test Symposium (1997) 296-301. (No month)
		J.B. Brockman & S.W. Director, "Predictive Subset Testing: Optimizing IC Parametric Performance Testing for Quality, Cost and Yield," IEEE Transactions on Semiconductor Manufacturing, Vol. 2 (1989) 104-113. (No month)
		W. Maly & Z. Pizlo, "Tolerance Assignment for IC Selection Tests," IEEE Transactions on Computer-Aided Design (April 1985) 156-162
		T.M. Souders & G.N. Stenbakken, "Cutting the High Cost of Testing," IEEE Spectrum (March 1991) 48-51
		S.D. Huss & R.S. Gyurcsik, "Optimal Ordering of Analog IC Tests to Minimize Time," Proceedings, Design Automation Conference (1991) 494-499. (No month)
		L. Milor & A.L. Sangiovanni-Vincentelli, "Minimizing Production Test Time to Detect Faults in Analog Circuits," IEEE Transactions on Computer-Aided Design, Vol. 13 (1994) 796-813. (No month)
		M.J. Marlett & J.A. Abraham, "DC-IATP: An Iterative Analog Circuit Test Generation Program for Generating DC Single Pattern Tests," Proceedings, IEEE International Test Conference (1988) 839-845. (No month)
		G. Devarayanadurg & M. Soma, "Analytic Fault Modeling and Static Test Generation for Analog ICs," International Conference for Computer-Aided Design (1994) 44-47. (No month)
		W.M. Lindermeir, H.E. Graeb & K.J. Antreich, "Design Based Analog Testing by Characteristic Observation Inference," International Conference for Computer-Aided Design (1995) 620-626. (No month)
		C.Y. Pan & K.T. Cheng, "Implicit Functional Testing for Analog Circuits," VLSI Test Symposium (1996) 489-494. (No month)
		P.N. Variyam & A. Chatterjee, "Test Generation for Comprehensive Testing of Linear Analog Circuits Using Transient Response Sampling," International Conference on Computer-Aided Design (1997) 382-385. (No month)
		K.J. Antreich, H.E. Graeb & C.U. Wieser, "Circuit Analysis and Optimization Driven by Worst Case Distances," IEEE Transaction on CAD, Vol. 13 (1994) 57-71. (No month)
		D.G. Saab, Y.G. Saab & J.A. Abraham, "CRIS: A Test Cultivation Program for Sequential VLSI Circuits," Proceedings: International Conference on Computer-Aided Design (1992) 216-219. (No month)
		G. Devarayanadurg, P. Goteti & M. Soma, "Hierarchy Based Statistical Fault Simulation of Mixed-Signal ICs," International Test Conference (1996) 521-527. (No month)
		A. Basilevsky, "Statistical Factor Analysis and Related Methods, Theory and Applications," Wiley Series in Probability and Mathematics (1994), 44 pages. (No month)

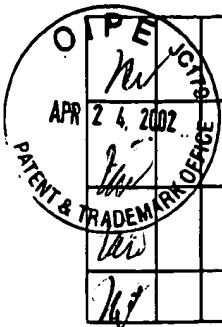
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09/837,887



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I.T. Jolliffe, "Discarding Variables in a Principle Component Analysis, I. Artificial Data," Applied Statistics, Vol. 22 (1973) 21-31. (No month)

APR 24, 2002
L. Milor & A.L. Sangiovanni-Vincentelli, "Optimal Test Set Design for Analog Circuits," International Conference on Computer-Aided Design (1990) 294-297. (No month)

A.V. Gomes & A. Chatterjee, "Minimal Length Diagnostic Tests for Analog Circuits Using Test History," Design, Automation and Test in Europe (1999) 189-194. (No month)

MATLAB Optimization Toolbox User's Guide, 4 pages. (No month)

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